Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please amend claims 1, 7 – 18, 20 - 22, inclusive, cancel claim 19, and add new claims 12 – 20, as follows:

Listing of Claims:

1 (Currently Amended). An integrated circuit comprising:

a plurality of computational elements; ~~elements including a plurality of arithmetic nodes, a plurality of bit-manipulation nodes, a plurality of finite state machine nodes, and a plurality of input/output nodes;~~

a first and a second processing node each having a core processor with a ~~based on a~~ common architecture, wherein the common architecture is configurable in response to a first configuration command to be a control node adapted to control an interconnection of said computational elements to perform a selected task and configurable in response to a second configuration command to be a programmable scalar node (PSN) adapted to perform a computational application;

a first memory associated with said first processing node;

a second memory associated with said second processing node;

a first interface ~~node wrapper for~~ coupling said core processor of said first processing node to said first memory and to said computational elements;

a second interface ~~node wrapper for~~ coupling said core processor of said second processing node to said second memory and to said computational elements, the first interface and the second interface having the same architecture. ~~; and~~

~~means for interconnecting said computational elements and said first and second processing nodes to define a selected task to achieve a desired functionality.~~

2 (Original). The integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function.

3 (Original). The integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least said first memory.

4 (Original). The integrated circuit of claim 3 wherein said executable code is downloaded from the Internet by said first processing node.

5 (Original). The integrated circuit of claim 4 wherein said executable code comprises operating system code.

6 (Original). The integrated circuit of claim 5 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function.

7 (Currently Amended). The integrated circuit of claim 1 wherein said plurality of computational elements are adapted to form ~~include~~ a plurality of arithmetic nodes, a plurality of bit-manipulation nodes and a plurality of finite state machine nodes.

8 (Currently Amended). The integrated circuit of claim 1 further comprising ~~comprises~~ a plurality of said second processing nodes and an interconnection network. ~~nodes each of which is~~ the plurality of said second processing nodes coupled through the interconnection network to said first processing node and plurality of computational elements. ~~elements by said interconnecting means.~~

9 (Currently Amended). An integrated circuit ~~adaptive computing engine~~ comprising:

a ~~controller~~ first node having:

a first core processor configurable in response to a first configuration signal into a controller node for execution of operating system code; ~~for executing operating system code~~;

a first memory for storing operating system executable code;

means for transferring operating system executable code and data from said first memory to said first core processor;

a plurality of computational elements adapted to perform a selected function; ~~function at least one of said computational elements having:~~

a ~~RISC~~ second node ~~processor~~ having:

a second core processor having the same circuit architecture as the first core processor, the second core processor ~~for~~ configurable into a RISC processor for execution of application code; ~~executing code;~~

a second memory for storing ~~executable~~ application code;

means for transferring ~~executable~~ application code and data from said memory to said ~~RISC~~ second core processor; ~~and~~

an interconnection network ~~a temporal interconnecting matrix~~ coupling said controller node and said RISC processor to said plurality of computational elements to perform the selected function; ~~a user selected function.~~

a first interface coupling said first core processor to said interconnection network; and

a second interface coupling said second core processor to said interconnection network, the first and second interfaces having a common interface architecture.

10 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 9 wherein said ~~controller~~ first node further comprises a configuration register, said configuration register containing a bit for determining whether said ~~controller~~ first node functions as ~~a~~ the controller node or as a RISC processor.

11 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 10 wherein said configuration register bit, when set, protects a portion of memory from access by said computational elements. ~~elements when set.~~

12 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 10 further comprising a protected portion of memory accessible only to said controller node.

13 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 9 wherein said ~~controller~~ first node and said second node further comprise: ~~further comprises:~~

an interface comprising: ~~a node wrapper having:~~

a data distributor for receiving an input stream from an external source, said input stream having configuration information, application code or ~~and~~ executable code;

a hardware task manager for receiving configuration information from said data distributor;

a DMA engine for receiving data and executable code from said data distributor;

a controller for providing said interface access to ~~node wrapper access~~ a set of registers associated with ~~said~~ the corresponding first or second core processor; and

an interrupt controller for detecting an interrupt condition. ~~interrupt conditions from said node wrapper and internally; and~~

~~a JTAG port associated with a debug register for debugging erroneous operation of said controller node.~~

14 (Currently Amended). An integrated circuit ~~adaptive computing engine~~ having a plurality of computational elements and an interconnection network for interconnecting a ~~temporal interconnecting matrix for connecting~~ said computational elements, said integrated circuit ~~adaptive computing engine~~ comprising:

a controller node ~~for adapting said computational elements in response to perform a selected function, said controller node~~comprising: ~~having:~~

a first core processor for executing operating system code;

a first memory for storing operating system executable code; and

~~means for transferring operating system executable code and data from said memory to said core processor;~~

~~a set of registers associated with said core processor;~~

a first interface ~~a node wrapper,~~ coupled to said first core processor and to the interconnect network ~~core processor,~~ for receiving and transferring to the first core processor a portion of an input stream from an external source, said input stream having configuration information or executable code; and

a programmable scalar node comprising:

a second core processor for executing instructions, the second core processor having the same circuit architecture as the first core processor;

an instruction memory for storing said instructions;

a data memory;

a second interface coupled to said second core processor and to the interconnection network for receiving an input stream from the controller node, said input stream having configuration information.

~~and executable code and passing said information to said core processor; and~~

~~means for accessing said set of registers;~~

~~an interrupt controller for detecting interrupt conditions from said node wrapper and internally.~~

15 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 14 further comprising means for accessing said first core processor and said first memory to debug error conditions.

16 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 14 further comprising means for ~~handling~~ node-to-node communication.

17 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 14 further comprising a second memory for storing executable code for controlling the ~~temporal adaptation of~~ interconnection of said computation elements in response to configuration information.

18 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 17 further comprising means for controlling an ~~the~~ initiation of operation of said computational element upon reset or power on.

19 (Canceled).

20 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 19 further comprising:

a data cache; and

an instruction cache.

21 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 20 further comprising a memory arbitration unit for managing access to said data memory and said instruction memory.

22 (Currently Amended). The integrated circuit ~~adaptive computing engine~~ of claim 14 further comprising means for controlling ~~minimizing~~ power consumption.

23 (New). The integrated circuit of claim 1, wherein the control node is configured to change the interconnecting of said computational elements and said first and second processing nodes to define a second task to achieve a second function previously not available or existent.

24 (New). The integrated circuit of claim 1, wherein the PSN node is a RISC processor.

25 (New). The integrated circuit of claim 9, wherein the controller node is configured to change the interconnection network coupling said controller node to said computational elements to perform a second selected function previously not available or existent.